REMARKS/ARGUMENTS

Claims 8, 12, 14, 16, and 18 are pending in this application. By this Amendment, Applicant AMENDS claims 8, 12, and 16 and CANCELS claims 9-11, 13, 15, 17, and 19.

Claims 8-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Sawada et al. (U.S. 5,412,601).

Claims 9-11, 13, 15, 17, and 19 have been canceled. Applicant respectfully traverses the rejection of claims 8, 12, 14, 16, and 18.

Claim 8 has been amended to recite:

> A semiconductor device comprising:
> a high voltage production circuit that produces a high voltage; and
> **a high voltage waveform conversion circuit provided at a subsequent stage of the high voltage production circuit that gradually outputs a high voltage by converting the waveform of the high voltage of the high voltage production circuit, the high voltage waveform conversion circuit including a delay circuit that delays the high voltage of the high voltage production circuit, and a voltage conversion switching element that lowers the delayed high voltage by a predetermined value**; and
> a memory cell in which data rewriting is performed by using the high voltage output by the high voltage waveform conversion circuit. (emphasis added)

With the unique combination and arrangement of features recited in Applicant's claim 8, including the features of "a high voltage waveform conversion circuit provided at a subsequent stage of the high voltage production circuit that gradually outputs a high voltage by converting the waveform of the high voltage of the high voltage production circuit", "the high voltage waveform conversion circuit including a delay circuit that delays the high voltage of the high voltage production circuit, and a voltage conversion switching element that lowers the delayed high voltage by a predetermined value", and "a memory cell in which data rewriting is performed by using the high voltage output by the high voltage waveform conversion circuit", Applicant has been able to provide a memory device that allows the stress acting on the memory cell to be alleviated (see, for example, paragraph [0007] of Applicant's substitute specification).

The Examiner alleged that Sawada et al. teaches all of the features recited in

Applicant's claims 8-10, including a high voltage production circuit 119 "that gradually outputs a high voltage by converting the waveform of the high voltage" and a delay circuit "that delays the high voltage of the high voltage production circuit, and a voltage conversion switching element that lowers the delayed high voltage by a predetermined value (col. 14, lines 16+; also see figures 2-3)."

Applicant has amended claim 8 to recite the features of "the high voltage waveform conversion circuit including a delay circuit that delays the high voltage of the high voltage production circuit, and a voltage conversion switching element that lowers the delayed high voltage by a predetermined value" and "a memory cell in which data rewriting is performed by using the high voltage output by the high voltage waveform conversion circuit." Support for these features is found, for example, in original claims 9 and 10.

First, Sawada et al. does not teach or suggest anything at all about a high voltage waveform conversion circuit *gradually* outputting a high voltage by converting the waveform of the high voltage. The Examiner alleged that the high voltage converter HVSW' in Fig. 4 of Sawada et al. gradually outputs a high voltage. However, as shown at the bottom of Fig. 5 of Sawada et al., the high voltage converter HVSW' sharply increases the voltage at the output terminal VPRG from 0 V to 22 V (see, for example, column 15, lines 62-68 of Sawada et al.). See also, for example, Applicant's Fig. 3 which compares the sharp increase in the voltage "a" of the prior art to the gradual increase in the voltage "b" of the presently claimed invention.

Second, Sawada et al. does not teach or suggest anything at all about a delay circuit that *delays* the high voltage of the high voltage production circuit 119. In the first full paragraph on page 3 of the outstanding Office Action, the Examiner appears to allege that column 14, lines 16+ and Figs. 2 and 3 of Sawada et al. teach a delay circuit. However, Sawada et al. does not remotely teach or suggest that the high voltage waveform conversion circuit HSVW' includes a delay circuit that delays the high voltage of the high voltage production circuit. The Examiner is respectfully requested to specifically point out where Sawada et al. teaches such a delay circuit.

Lastly, Sawada et al. does not teach a voltage conversion switching element that *lowers* the delayed high voltage by a predetermined value. Sawada et al. merely discloses that the program circuit 120 can select a program voltage from four values (see, for example, column 8, lines 42-49 of Sawada et al.) using the capacitors C1-C4 (see, for example, column 10, lines 12-43 of Sawada et al.). The program circuit 120 of Sawada et al. does not include a voltage conversion switching element that *lowers* the high voltage from the high voltage generation control circuit 119, but instead determines the voltage using capacitors. In fact, in most instances, the program circuit 120 of Sawada et al. actually *increases* the voltage (see, for example, the sentence bridging columns 7 and 8 and column 8, lines 45-48 of Sawada et al.).

Thus, Sawada et al. clearly fails to teach or suggest the features of "a high voltage waveform conversion circuit provided at a subsequent stage of the high voltage production circuit that gradually outputs a high voltage by converting the waveform of the high voltage of the high voltage production circuit", "the high voltage waveform conversion circuit including a delay circuit that delays the high voltage of the high voltage production circuit, and a voltage conversion switching element that lowers the delayed high voltage by a predetermined value", and "a memory cell in which data rewriting is performed by using the high voltage output by the high voltage waveform conversion circuit," as recited in Applicant's claim 8.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 8 under 35 U.S.C. § 102(b) as being anticipated by Sawada et al.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claim 8 is allowable. Claims 12, 14, 16, and 18 depend upon claim 8, and are therefore allowable for at least the reasons that claim 8 is allowable.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicant petitions the Commissioner for a ONE-month extension of time, extending to June 16, 2008 (June 14, 2008 falls on a Saturday), the

period for response to the Office Action dated February 14, 2008.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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